In the Claims

1. (currently amended) ~~An arbitration throttling control~~ circuit ~~for use in disc drive to self throttle data transfer of an error correction buffer in a disc drive, arbitration throttling control circuit~~ comprising:

~~an error correction buffer~~ a first buffer interface that monitors availability of data from ~~the error correction~~a first buffer;

a ~~disc drive main buffer memory~~ second buffer interface that controls data transfer from the ~~error correction~~first buffer to a ~~disc drive main~~second buffer ~~memory~~ in a plurality of data bursts, each data burst having a predetermined burst quantity of data; and

a control circuit, ~~operatively~~ coupled to the ~~error correction buffer~~ interfaces ~~and to the disc drive main buffer memory interface,~~ that arbitrates for access to transfer data into the ~~disc drive main~~second buffer ~~memory~~ such that a series of data bursts totaling a predetermined ~~sector~~ quantity of data from the ~~error correction~~first buffer to the ~~disc drive main~~second buffer ~~memory~~ is spread substantially evenly over a period of time substantially equal to a transfer time of the ~~sector~~ predetermined quantity of data into the ~~error correction~~first buffer, wherein the ~~sector~~ predetermined quantity of data is larger than the burst quantity of data.

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2. (currently amended) The ~~arbitration throttling control~~ circuit of claim 1, wherein the ~~control~~ circuit, upon an indication that the ~~sector~~ predetermined quantity of data from the ~~error correction~~first buffer is available for transfer, provides one arbitration request to obtain data transfer access to the ~~disc drive main~~second buffer ~~memory~~ from the ~~error correction~~first buffer ~~for each time period substantially equal to a time needed for a burst quantity of data to be transferred from the disc~~.

3. (currently amended) The ~~arbitration throttling control~~ circuit of claim 1, wherein the ~~sector~~ predetermined quantity of data includes (512) data bytes, each one of the data bursts of the burst quantity of data includes sixty-four data bytes, and ~~the~~ a buffer controller enables up to one additional data burst to occur each time period substantially equal to a time needed for sixty-four data bytes to be transferred from the disc.

4. (currently amended) The ~~arbitration throttling control~~ circuit ~~system~~ of claim 3~~1~~, wherein the buffer controller further comprises:

a byte-clock counter that is clocked based on a frequency of data transfer from the disc, and that produces an output pulse based on the byte-clock counter counting a predetermined number of clock cycles:

an arbitration request counter, operatively coupled to the byte-clock counter, that is incremented by the output pulse of the byte-clock counter, that is decremented when a disc-channel arbitration grant is obtained, and that produces a disc-channel arbitration request if the arbitration request counter has a value of one or more; and

an arbitration logic, operatively coupled to the arbitration request counter, that receives disc-channel arbitration requests and provides disc-channel arbitration grants, in order to spread data bursts from the error-correction buffer to the disc- drive main buffer memory over a period of time substantially equal to the sector transfer time.

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5. (currently amended) The ~~arbitration throttling control~~ circuit of claim 4, wherein the buffer controller further comprises:

a reset circuit configured to reset the byte-clock counter based on a data availability of data out of the error-correction buffer.

6. (currently amended) The ~~arbitration throttling control~~ circuit of claim 4, wherein each one of the data bursts includes N data bytes, and the arbitration request counter is incremented once for each N byte-clock cycles.

7. (currently amended) The ~~arbitration throttling control~~ circuit of claim 4, wherein a sector transfer includes (512) data bytes, each one of the data bursts includes sixty-four data bytes, and the arbitration request counter is incremented once for each time period substantially equal to a time needed for sixty-four data bytes to be transferred from the disc.

8. (currently amended) An apparatus~~disc drive system~~ comprising:

~~a disc case;~~

~~a disc rotatably mounted within the disc case;~~

~~an actuator assembly mounted within the disc case, the actuator assembly having a transducer head in transducing relationship to the disc;~~

~~an error correction buffer operatively~~a first data store coupled to receive data ~~from the transducer head~~ at a ~~disc~~ first data rate.~~;~~

~~a disc drive main buffer memory operatively coupled to receive data from the error correction buffer in a plurality of data bursts, each data burst having a burst data rate higher than the disc data rate and each data burst transferring a burst predetermined quantity of data;~~

~~a system interface;~~

~~a disc drive controller operatively coupled to transfer data from the disc drive main buffer memory to the system interface; and~~

~~an arbitration throttling control circuit that arbitrates for access to~~ wherein the apparatus is configured to transfer ~~data into the disc drive main buffer memory such that~~ data bursts totaling an amount ~~sector quantity~~ of received data from the ~~error correction buffer to the disc drive main buffer memory~~first data store that are spread substantially evenly over a period of time substantially equal to a transfer time of the ~~sector~~ predetermined quantity of data ~~from the disc~~ into the first data store~~error correction buffer~~, wherein the ~~sector quantity~~ amount of received data is larger than the burst quantity of data.

9. (currently amended) The ~~disc drive system~~apparatus of claim 8 further comprising:

an arbitration-throttling control circuit; and

a second data store, wherein the arbitration-throttling control circuit, upon an indication that the ~~sector quantity~~ amount of received data from the ~~error correction buffer~~first data store is available for transfer, provides one arbitration request to obtain data transfer access to the ~~disc drive main buffer memory~~second data store from the ~~error correction buffer~~first data store for each time period substantially equal to a time needed for the burst quantity of data to be transferred ~~from the disc~~.

10. (currently amended) The ~~disc-drive system~~apparatus of claim ~~8~~9, wherein the ~~sector quantity~~ amount of received data includes (512) data bytes, each one of the data bursts of the burst quantity of data includes sixty-four data bytes, and the arbitration-throttling control circuit enables up to one additional data burst to occur each time period substantially equal to a time needed for sixty-four data bytes to be transferred from ~~the~~ a storage medium~~disc~~.

11. (currently amended) The ~~disc-drive system~~apparatus of claim ~~8~~9, wherein the arbitration-throttling control circuit further comprises:

a byte-clock counter that is clocked based on a rate of data transfer from the storage medium~~disc~~, and that produces an output pulse based on the byte-clock counter counting a predetermined number of clock cycles;

an arbitration request counter, operatively coupled to the byte-clock counter, that is incremented by the output pulse of the byte-clock counter, that is decremented when a disc-channel arbitration grant is obtained, and that produces a disc-channel arbitration request if the arbitration request counter has a value of one or more; and

an arbitration logic, operatively coupled to the arbitration request counter, that receives disc-channel arbitration requests and provides disc-channel arbitration grants, in order to spread data bursts from the ~~error-correction buffer~~first data store to the ~~disc-drive main buffer memory~~ second data store over a period of time substantially equal to the ~~sector~~ transfer time of the received data.

12. (currently amended) The ~~disc-drive system~~ apparatus of claim 11, wherein the arbitration-throttling control circuit further comprises:

a reset circuit configured to reset the byte-clock counter based on a data transfer count of data out of the ~~error-correction buffer~~first data store.

13. (currently amended) The ~~disc-drive system~~apparatus of claim 11, wherein each one of the data bursts includes N data bytes, and the arbitration request counter is incremented once for each N byte-clock cycles.

14. (currently amended) The ~~disc drive system~~apparatus of claim 11, wherein a sector transfer includes (512) data bytes, each one of the data bursts includes sixty-four data bytes, and the arbitration request counter is incremented once for each time period substantially equal to a time needed for sixty-four data bytes to be transferred from the disc.

15. (currently amended) The ~~disc drive system~~ apparatus of claim 11, further comprising:

a data-handling system operatively coupled to at least read data from the disc, the data-handling system further comprising:

one or more data processors;

one or more memories operatively coupled to each one of the one or more data processors; and

at least one input/output system coupled to at least one of the one or more data processors to receive input data and to supply output data.

16. (currently amended) A method ~~for self-throttling data transfer in an error-correction buffer in a disc drive, the method~~ comprising steps of:

(a) receiving data into ~~the error-correction~~a first buffer ~~from a disc transducer~~ at a ~~disc~~ first data rate; and

(b) transferring the data out of the ~~error-correction~~first buffer in a plurality of data bursts, each one of the data bursts having a burst data rate that is higher than the ~~disc~~ first data rate, the data bursts having a ~~spacing based on a~~ timing ~~signal derived from~~ based on the ~~disc~~ first data rate.

17. (currently amended) The method according to claim 16, further comprising a step of:

(c) performing an error correction operation on the data within the ~~error-correction~~ first buffer before performing the transferring step (b).

19 18. (currently amended) The method according to claim 17 16, wherein the transferring step (b) further comprises:

(b)(i) deriving a burst-enable pulse by dividing a clock signal by a predetermined value, wherein the clock signal is based on the ~~disc~~ first data rate, and the predetermined value is based on an amount of data in one of the plurality of data bursts.

20 19. (currently amended) The method according to claim 17 16, wherein the transferring step (b) further

comprises:

(b)(ii) upon an indication that the sector quantity of data from the ~~error-correction~~ first buffer is available for transfer, providing an arbitration request to obtain data transfer access to ~~the disc drive main~~a second buffer ~~memory~~ from the ~~error-correction~~first buffer for each time period substantially equal to a time needed for a burst quantity of data to be transferred ~~from the disc~~.

21 20. (original) A disc drive system comprising:

a base plate;

a rotatable disc mounted to the base plate;

an actuator, the actuator including a transducer mounted to the actuator in transducing relation to the disc:

buffer memory means operatively coupled to the transducer for self-throttling data bursts of an error-correction buffer.

16 21. (new) The apparatus of claim 8 further comprising a second data store coupled to receive the data bursts from the first data store, each data burst having a burst data rate higher than the first data rate.